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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DUNCAN, MARC M	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/965,883	MAJNI ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-15* is/are rejected.

7)☒ Claim(s) *7-9,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/7/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Imbert de Tremiolles et al. (hereinafter Imbert).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert in view of Microsoft.

Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert in view of Olarig et al.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert and Microsoft as applied to claim 11 above, and further in view of Olarig et al.

Claims 7-9 and 16-17 are objected to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Imbert de Tremiolles et al. (hereinafter Imbert).

Regarding claim 1:

Imbert teaches a host/data controller in Fig. 1 – "120."

Imbert teaches a memory system comprising a plurality of memory cartridges operably coupled to the host/data controller, each memory cartridge comprising an operation indicator configured to indicate the operational status of the corresponding memory cartridge in Fig. 1, Fig. 3 and col. 4 lines 23-33 and lines 40-41.

Regarding claim 10:

Imbert teaches wherein each of the plurality of memory cartridges comprises a plurality of memory devices in Fig. 1 and col. 3 line 67-col. 4 line 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert in view of Microsoft.

Regarding claim 11:

Imbert teaches detecting an error in a memory subsystem in col. 4 lines 17-18.

Imbert teaches determining the operational status of the memory system in col. 4 lines 23-33 and lines 40-41.

Imbert does not explicitly teach initiating a system interrupt signal. Imbert does, however, teach taking different actions depending on whether a hard or soft error was detected, these actions including notifying the controller of the hard error and changing the status of a cartridge in the card assignment table in col. 4 lines 23-33.

Microsoft teaches initiating system interrupt signals in the definition of interrupt.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the interrupts of Microsoft with the error detection and notification of Imbert.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Imbert includes an explicit and inherent need to notify the controller of errors. The interrupt signals of Microsoft meet this need of Imbert. Interrupt signals are used to notify the processor or controller of problems (see definition of interrupt - lines 8-9).

Regarding claim 12:

Imbert teaches wherein the act of detecting an error comprises the act of detecting a multi-bit error in col. 1 lines 53-54. The utilization of Block Error Code necessarily includes the ability to detect and correct multi-bit errors.

Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert in view of Olarig et al.

Regarding claim 2:

The teachings of Imbert are outlined above.

Imbert does not explicitly teach wherein the memory system comprises a redundant memory system. Imbert does however, teach that it would be desirable to increase the availability and reliability of the memory system of the computer in col. 2 lines 9-10.

Olarig teaches a memory system comprising a redundant memory system in col. 5 lines 55-63.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the redundant memory system of Olarig with the memory system of Imbert.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Olarig teaches that the redundant scheme outlined in Olarig provides a fault tolerant, i.e. reliable, memory system, thus meeting an explicitly stated desire and need of Imbert without necessitating the use of extra memory modules.

Regarding claim 3:

Olarig teaches wherein the memory system comprises five memory cartridges in Fig. 2. Olarig pictures a plurality of memory cartridges. Five memory cartridges are, therefore, implicitly taught.

Regarding claim 4:

Imbert teaches wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational

and the second state indicating that the memory cartridge is not operational in col. 4 lines 23-33 and lines 40-41.

Regarding claim 5:

Olarig teaches wherein the memory system is configured to operate in a redundant mode when each of the bits is in the first state in col. 1 lines 39-46 and col. 9 lines 55-63. When the memory module is powered and the connector is live, the memory module is used in a redundant, fault tolerant scheme. If each of the bits is in the first state, i.e. none of the cartridges has failed and must be replaced, each cartridge is connected and live and is used in a redundant, fault tolerant scheme.

Regarding claim 6:

Imbert teaches wherein at least one of the host/data controller and the plurality of memory cartridges comprise error detection components in Fig. 2A and 2B and col. 4 lines 17-18.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imbert and Microsoft as applied to claim 11 above, and further in view of Olarig et al.

Regarding claim 13:

The teachings of Imbert and Microsoft are outlined above.

Imbert and Microsoft do not explicitly teach a redundant memory system and therefore determining whether the system is operating in one of a redundant and non-redundant mode. Imbert and Microsoft do, however, teach that it would be desirable to increase the availability and reliability of the memory system of the computer in Imbert, col. 2 lines 9-10.

Olarig teaches a redundant memory system in col. 5 lines 55-63. The combination of the redundant memory system of Olarig with the system of Imbert and Microsoft results in a system that determines whether the system is operating in one of a redundant and a non-redundant mode. In Imbert and Microsoft, checking the operational status comprises checking whether any of the memory cartridges has failed. In Olarig, if a memory cartridge has failed the system operates in a non-redundant mode and if no cartridges have failed the system operates in a redundant mode. It can clearly be seen that in the combination of Olarig with Imbert and Microsoft, checking the operational status clearly comprises checking whether the system is operating in a redundant or non-redundant mode.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the redundant system of Olarig with the memory system of Imbert and Microsoft.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Olarig teaches that the redundant scheme outlined in Olarig provides a fault tolerant, i.e. reliable, memory system, thus meeting an explicitly stated desire and need of Imbert without necessitating the use of extra memory modules.

Regarding claim 14:

Imbert teaches wherein the act of determining the operational status comprises reading a plurality of operation bits, each of the operation bits indicating the operational status of a corresponding segment of the memory, the operational status comprising

one of an operational state and a non-operational state in col. 4 lines 23-33 and lines 40-41 and col. 5 lines 34-37.

Regarding claim 15:

The combination teaches wherein the act of determining the operational status comprises reading five operation bits. This limitation is inherent to the combination of Imbert, Microsoft and Olarig. It has been shown in the citations above that the system of the combination comprises five memory cartridges. Each memory cartridge has an associated operation bit. It has also been shown in the citations above that determining the operational status comprises reading each of the operation bits. It is, therefore, necessarily true that determining the operational status comprises reading five operation bits.

Allowable Subject Matter

Claims 7-9 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests initiating a low priority interrupt if each of the operation bits is in the first state as outlined in claims 7, 8 and 16. Prior art was not found that explicitly teaches or fairly suggests initiating a high priority interrupt if each of the operation bits is in the second state as outlined in claims 9 and 17.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art not relied upon contains elements of the instant claims and/or represents a current state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

SCOTT BADERMAN
PRIMARY EXAMINER